the source voltage thereof.

3. (Amended) A semiconductor integrated circuit as set forth in claim 1, which further comprises a second capacitor element provided between the drain terminal and the source terminal of said FET,

wherein a capacitance value of said second capacitor element is set so that a parasitic resistance component of said FET decreases when the drain voltage of said FET is lower than the source voltage thereof.

4. (Amended) A semiconductor integrated circuit as set forth in claim 1, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to control a magnitude relationship between the drain voltage and the source voltage of said FET.

5. (Amended) A semiconductor integrated circuit as set forth in claim 2, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to control a magnitude relationship between the drain voltage and the source voltage of said FET.

6. (Amended) A semiconductor integrated circuit as set forth in claim 3, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to control a magnitude relationship between the drain voltage and the source voltage of said FET.

12. (Amended) A semiconductor integrated circuit as set forth in claim 11, which further comprises a second capacitor element provided between the gate terminal and the source terminal of said FET,

wherein a capacitance value of said second capacitor element is set so that a parasitic resistance component of said FET decreases when the drain voltage of said FET is lower than the source voltage thereof.